memory transistors formed in each of said memory regions to perform nonvolatile storage of data, each memory transistor including:

a floating gate which is formed on said semiconductor substrate via a first gate insulating layer,

a control gate which is formed on said floating gate via a second gate insulating layer, and is strip-shaped, said control gate extending in another direction perpendicular to said one direction, and said control gate being common to said memory transistors, and

two source/drain diffusion layers formed on the surface of said semiconductor substrate;

sidewalls formed of a first silicon nitride layer, and covering both sides of said floating gate and said control gate of each of said memory transistors, said sidewalls being formed via an oxide layer serving as a stopper at the time of the etching for forming said sidewalls; and

layers formed of a second silicon nitride layer each covering at least upper surfaces of said control gate and surfaces of said sidewalls of each of said transistors, said each layer being removed by etching so as not to exist on said source/drain diffusion layers, so that the source/drain diffusion layers are exposed. --

-- 19. (NEW) The nonvolatile semiconductor memory device according to claim 18, further comprising silicide layers formed on the surfaces of said control gate and said source/drain diffusion layers in each of said memory transistors. --

-- 20. (NEW) The nonvolatile semiconductor memory device according to claim 19, wherein in each of said memory transistors, one of the two source/drain diffusion layers is connected to a bit line via said silicide layer, and the other is connected to a common source line via said silicide layer. --

-- 21. (NEW) The nonvolatile semiconductor memory device according to claim 18, further comprising at least one of a low-voltage MOS transistor and a high-voltage MOS transistor formed as a periphery circuit. --

Cont
FIG 1